What is claimed is:

1. A spin-on glass composition for use in forming a silicon oxide layer during semiconductor manufacturing, said composition comprising:

perhydropolysilazane having the compound formula $-(SiH_2NH)_n-$ wherein n represents a positive integer, in an amount of about 10 to about 30% by weight, based on the total weight of the composition, whereby the perhydropolysilazane has a weight average molecular weight within the range of about 4,000 to 8,000 and a molecular weight dispersion within the range of about 3.0 to 4.0; and

a solvent in an amount of about 70-90% by weight, based on the total weight of the composition.

2. The spin-on glass composition as claimed in claim 1, wherein the weight average molecular weight of the perhydropolysilazne is about 6000-8000 when the silicon oxide layer is formed to fill a trench.

3. The spin-on glass composition as claimed in claim 1, wherein the weight average molecular weight of the perhydropolysilazne is about 4000-6000 when the silicon oxide layer is formed to planarize gate electrodes.

4. The spin-on glass composition as claimed in claim 1, wherein the weight average molecular weight of the perhydropolysilazne is about 4500-7500 when the silicon oxide layer is formed to planarize metal patterns.

5. The spin-on glass composition as claimed in claim 1, wherein the perhydropolysilazane is present in an amount of about 18-25% by weight, based on the total weight of the composition, and the solvent is present in an amount of about 75-82% by weight, based on the total weight of the composition.

6. The spin-on glass composition as claimed in claim 1, wherein the composition has a uniform viscosity within the range of about 1 to about 10 mPa.s at a shear rate within the range of about 54 to about 420 (1/s).

7. The spin-on glass composition as claimed in claim 1, wherein the composition has a contact angle of no more than about 4° with respect to an underlying layer on which the composition is coated.

8. The spin-on glass composition as claimed in claim 1, wherein the composition further comprises at least one impurity material selected from the group consisting of boron, fluorine, phosphorous, arsenic, carbon, oxygen, and mixtures thereof.

9. The spin-on glass composition as claimed in claim 1, wherein the solvent is selected from xylene or dibutyl ether.

10. A method of forming a silicon oxide layer comprising:

providing a semiconductor substrate having a stepped portion;

coating the semiconductor substrate with a spin-on glass (SOG) composition containing perhydropolysilazane having the compound formula $-(SiH_2NH)_n-$ wherein n represents a positive integer, a weight average molecular weight within the range of about 4,000 to about 8,000, and a molecular weight dispersion within the range of about 3.0 to about 4.0, and

curing the SOG layer to form a layer of silicon oxide having a planar surface.

11. The method as claimed in claim 10, wherein curing the SOG layer comprises:

pre-baking the SOG layer at a temperature within the range of about 100 to about 500°C for a first period of time; and

main-baking the SOG layer at a temperature within the range of about 400 to about 1,200°C for a second period of time.

12. The method as claimed in claim 11, wherein the main-baking is conducted under an atmosphere comprising one or more components selected from the group consisting of oxygen, water vapor, mixtures of oxygen and water vapor, nitrogen, and mixtures thereof, for about 10 to about 180 minutes.

13. The method as claimed in claim 10, wherein the spin-on glass composition has a uniform viscosity within the range of about 1 to about 10 mPa.s, at a shear rate within the range of about 54 to about 420 (1/s).

14. The method as claimed in claim 10, wherein the thickness of the silicon oxide layer is within the range of about 4,000 to about 6,500Å.

15. The method as claimed in claim 10, wherein the stepped portion is formed by at least two conductive patterns.

16. The method as claimed in claim 15, wherein the distance between the at least two conductive patterns is within the range of about 0.04 to about 1 μm.

17. The method as claimed in claim 15, wherein an aspect ratio of the stepped portion between at least two conductive patterns is within the range of about 5:1 to about 10:1.

18. The method as claimed in claim 15, wherein the stepped portions has an aspect ratio within the range of from about 5:1 to about 10:1, and a global stepped portion having an aspect ratio less than about 1:1.

19. The method as claimed in claim 15, wherein the at least two conductive patterns are selected from gate electrodes and metal wiring patterns of a semiconductor device.

20. The method as claimed in claim 10, further comprising forming a silicon nitride layer having a thickness within the range of about 200 to about 600Å on the semiconductor substrate before coating the spin-on glass composition.

21. The method as claimed in claim 20, wherein the spin-on glass solution has a contact angle of no more than about 4° with respect to the silicon nitride layer.

22. The method as claimed in claim 10, wherein the spin-on glass composition further comprises at least one impurity material selected from the group consisting of boron, fluorine, phosphorous, arsenic, carbon, oxygen, and mixtures thereof.

23. The method as claimed in claim 10, wherein the stepped portion is formed by:

partially etching an upper portion of the semiconductor substrate to form a trench; and

the silicon oxide layer is formed by;

coating the SOG composition on the substrate to fill the trench and to form an SOG layer; and

curing the SOG layer by:

pre-baking the SOG layer at a temperature within the range of about 100 to about 500°C for a first period of time; and

main-baking the SOG layer at a temperature within the range of about 900 to about 1000°C for a second period of time.

24. The method as claimed in claim 23, wherein the weight average molecular weight of the perhydropolysilazne of the SOG composition is about 6000-8000.

25. The method as claimed in claim 10, wherein the stepped portion is formed by:

forming a plurality of gate electrodes on the semiconductor substrate;

and the silicon oxide layer is formed by;

coating a SOG composition on the substrate to completely cover the plurality of gate electrodes and to form a SOG layer; and

curing the SOG layer by:

pre-baking the SOG layer at a temperature within the range of about 100 to about 500°C for a first period of time; and

main-baking the second SOG layer at a temperature within the range of from about 600 to about 900°C for a second period of time.

26. The method as claimed in claim 25, wherein the weight average molecular weight of the perhydropolysilazne of the SOG composition is about 4000-6000.

27. The method as claimed in claim 10, wherein the stepped portion is formed by:

forming an insulation layer on the semiconductor substrate; and

forming a plurality of metal wiring patterns on the insulation layer;

and the silicon oxide layer is formed by;

coating a SOG composition on the substrate to completely cover the metal wiring patterns thereby to form a SOG layer; and

curing the SOG layer by:

pre-baking the SOG layer at a temperature within the range of from about 100 to about 500°C for a first period of time; and

main-baking the third SOG layer at a temperature within the range of from about 400 to about 450°C for a second period of time.

28. The method as claimed in claim 27, wherein the weight average molecular weight of the perhydropolysilazne of the SOG composition is about 4500-7500.

29. A semiconductor device having at least one planar layer formed without performing a polishing process to attain planarization, the at least one planar layer comprising the composition of claim 1.

30. The semiconductor device as recited in claim 29, wherein the weight average molecular weight of the perhydropolysilazne is about 6000-8000 when the silicon oxide layer is formed to a fill trench.

31. The semiconductor device as recited in claim 29, wherein the weight average molecular weight of the perhydropolysilazne is about 4000-6000 when the silicon oxide layer is formed to planarize gate electrodes.

32. The semiconductor device as recited in claim 29, wherein the weight average molecular weight of the perhydropolysilazne is about 4500-7500 when the silicon oxide layer is formed to planarize metal patterns.

33. The semiconductor device as recited in claim 29, wherein the solvent comprises one of xylene and dibutyl ether.

34. The semiconductor device as recited in claim 29, wherein the mixture comprises about 18-25% by weight of perhydropolysilazane and about 75-82% solvent.

35. The semiconductor device as recited in claim 29, wherein the mixture has a viscosity of about 1 to 10 mPa.s and a shear rate of about 54 to 420 (1/s).

36. The semiconductor device as recited in claim 29, wherein the mixture has a contact angle of no more than about 4° with respect to an underlying layer on which the mixture is deposited.

37. The semiconductor device as recited in claim 29, wherein the mixture includes an impurity selected from the group including consisting of boron, florine, phosphorous, arsenic, carbon, oxygen, and a combination thereof.